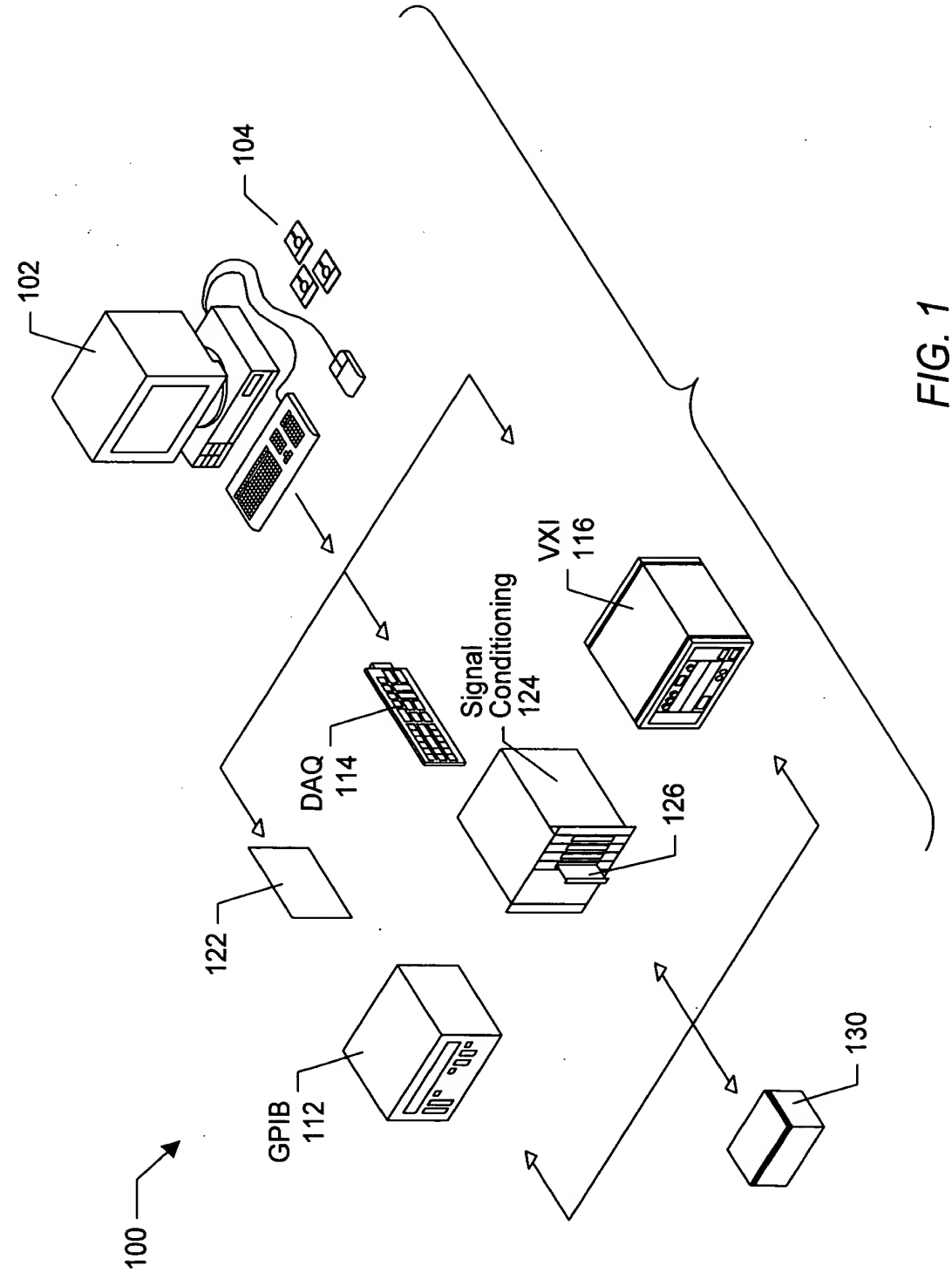

FIG. 1

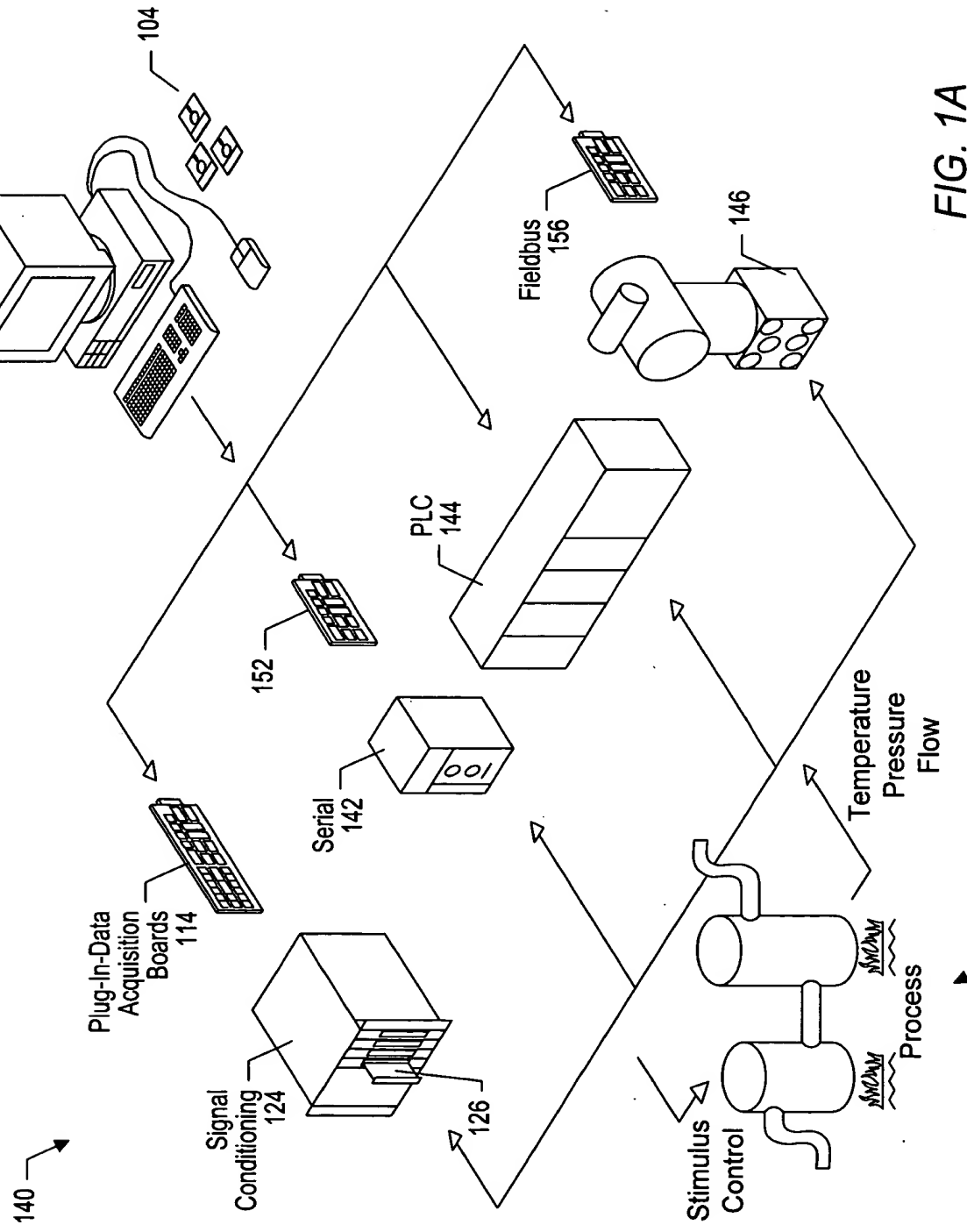
102
104
Fieldbus
156
146
PLC
144
152
Serial
142
Plug-In-Data
Acquisition
Boards
114
Signal
Conditioning
124
126
Temperature
Pressure
Flow
Process
160
Stimulus
Control
140

FIG. 1A

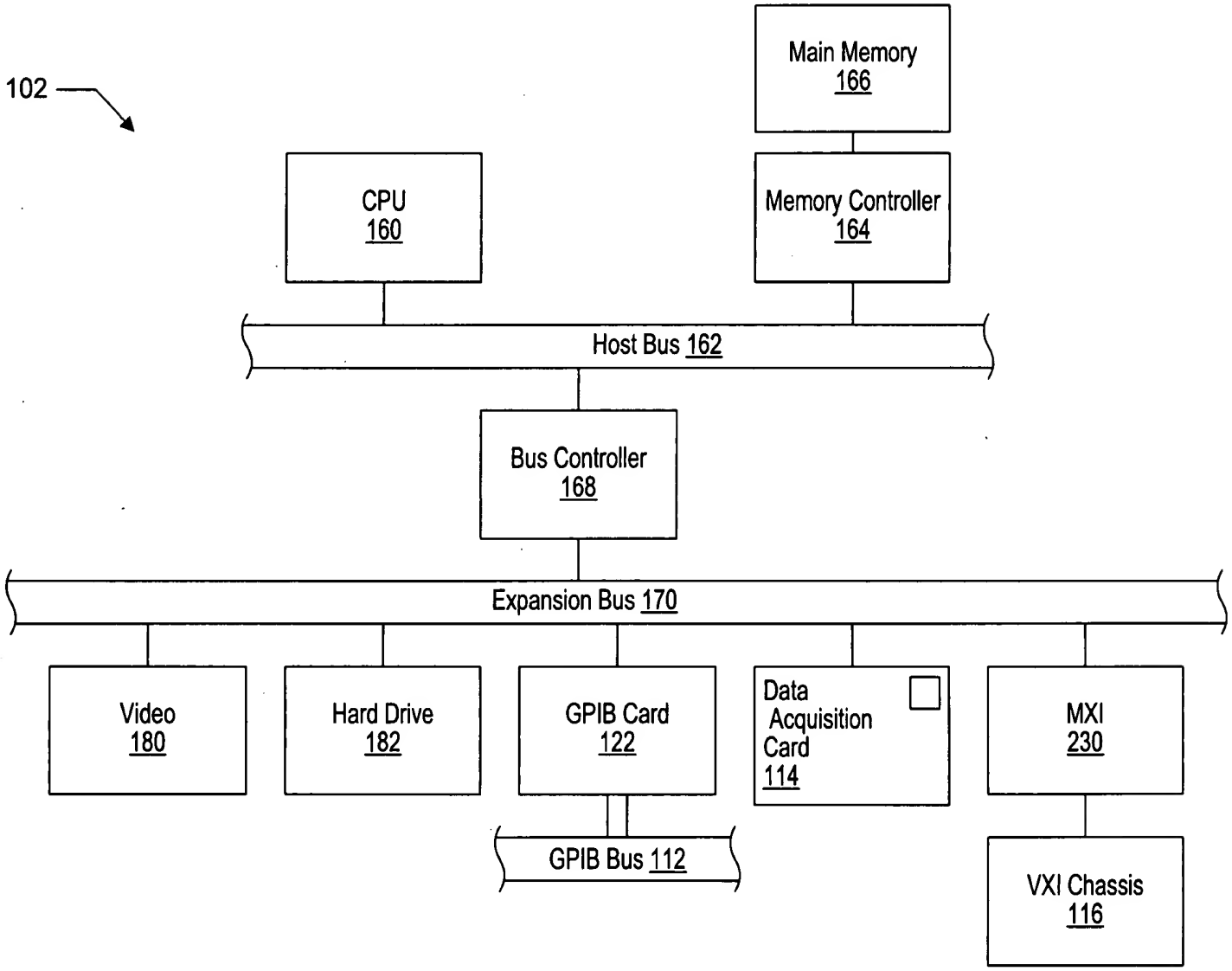

FIG. 2

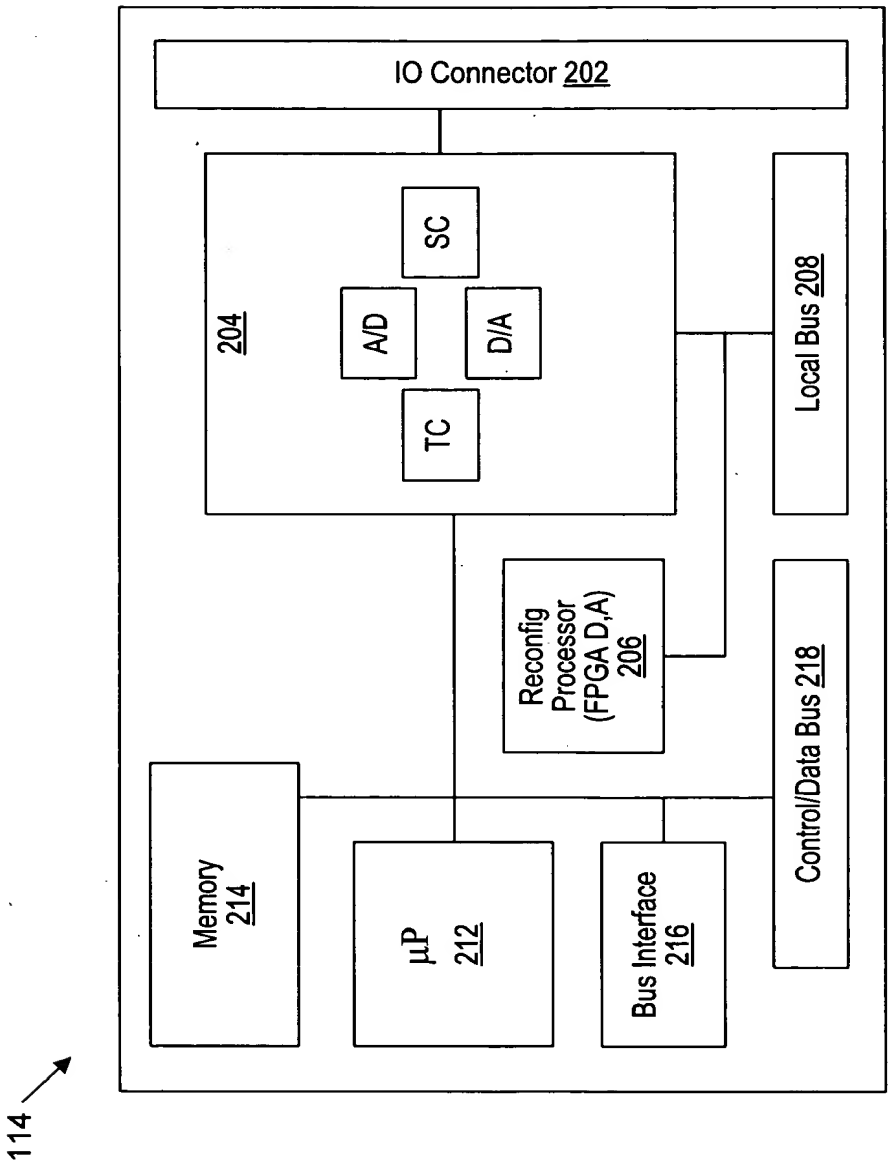
IO Connector 202
204
SC
A/D
D/A
TC
Local Bus 208
Reconfig Processor (FPGA D,A) 206
Control/Data Bus 218
Memory 214
µP 212
Bus Interface 216
114

FIG. 3

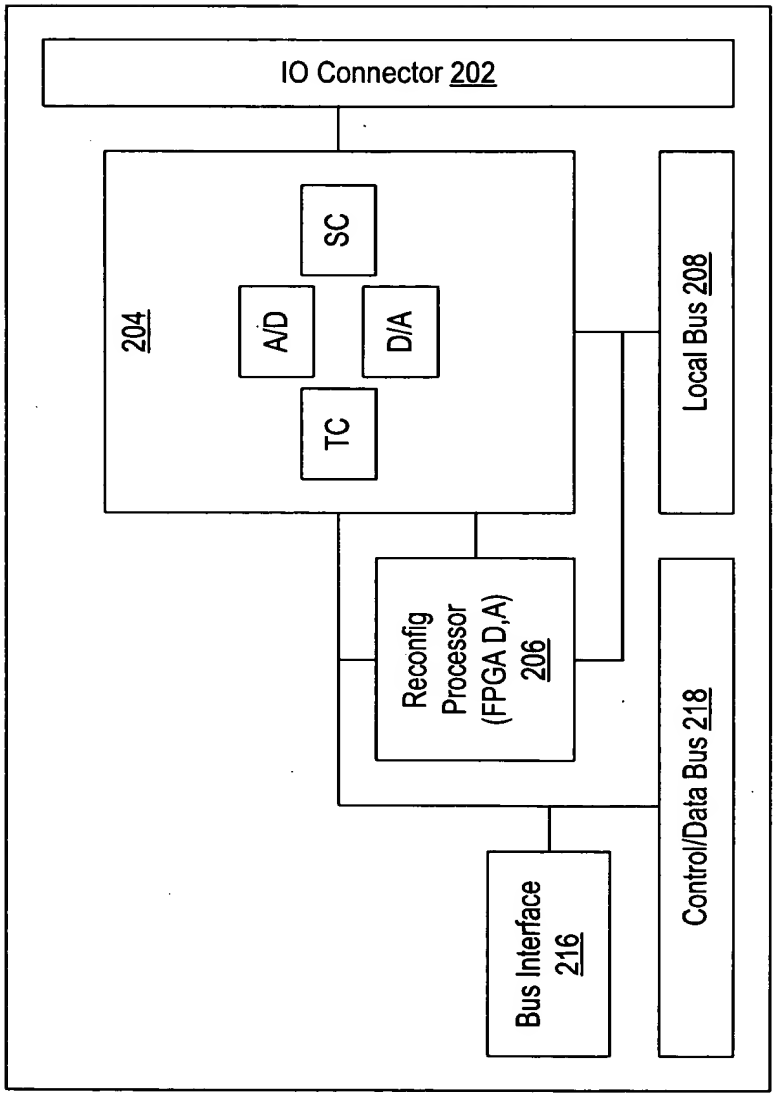
IO Connector 202
204
SC
A/D
D/A
TC
Local Bus 208
Reconfig Processor (FPGA D,A) 206
Bus Interface 216
Control/Data Bus 218

FIG. 3A

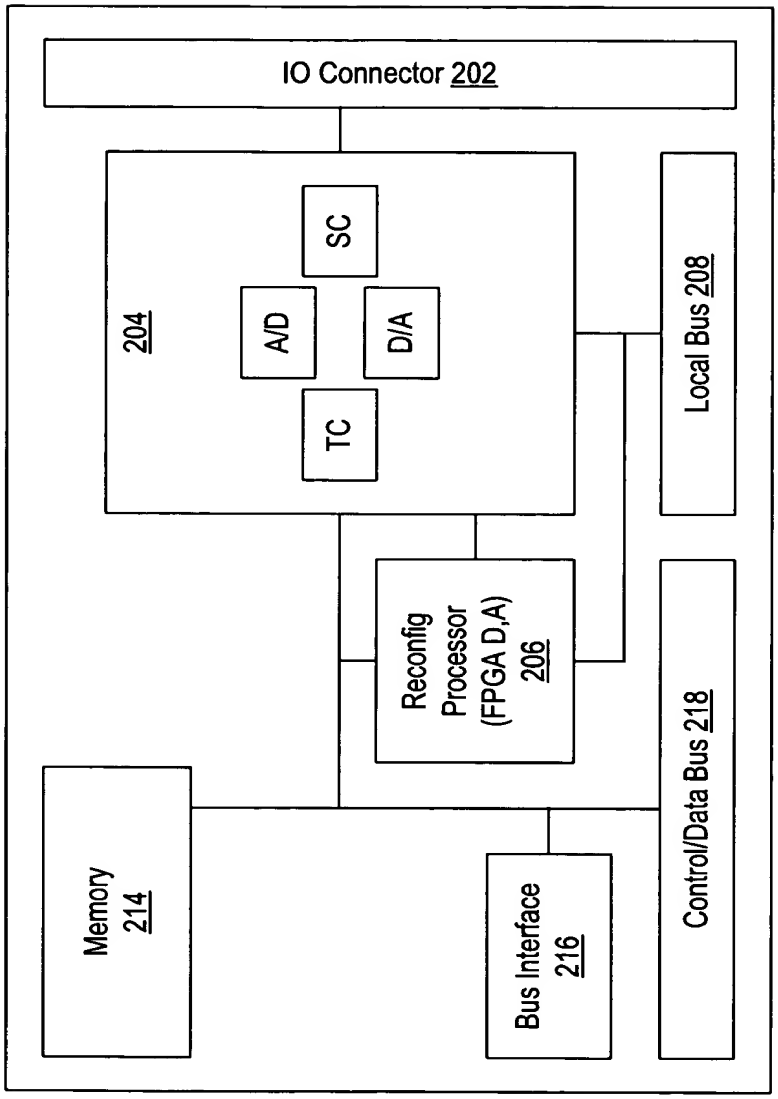
IO Connector 202
204
SC
A/D
D/A
TC
Local Bus 208
Reconfig Processor (FPGA D,A) 206
Memory 214
Bus Interface 216
Control/Data Bus 218

FIG. 3B

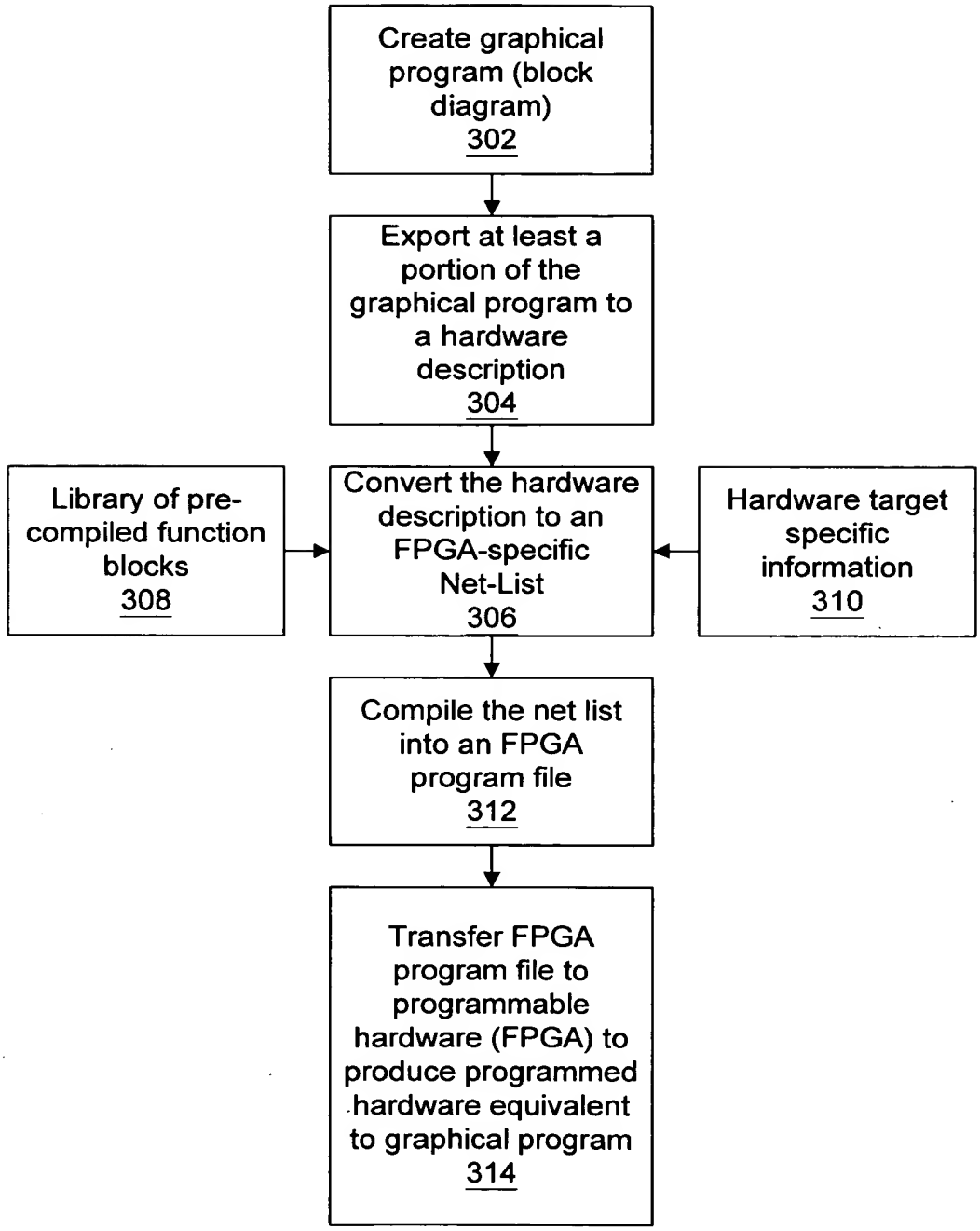
Create graphical program (block diagram) 302
Export at least a portion of the graphical program to a hardware description 304
Library of pre-compiled function blocks 308
Convert the hardware description to an FPGA-specific Net-List 306
Hardware target specific information 310
Compile the net list into an FPGA program file 312
Transfer FPGA program file to programmable hardware (FPGA) to produce programmed hardware equivalent to graphical program 314

FIG. 4

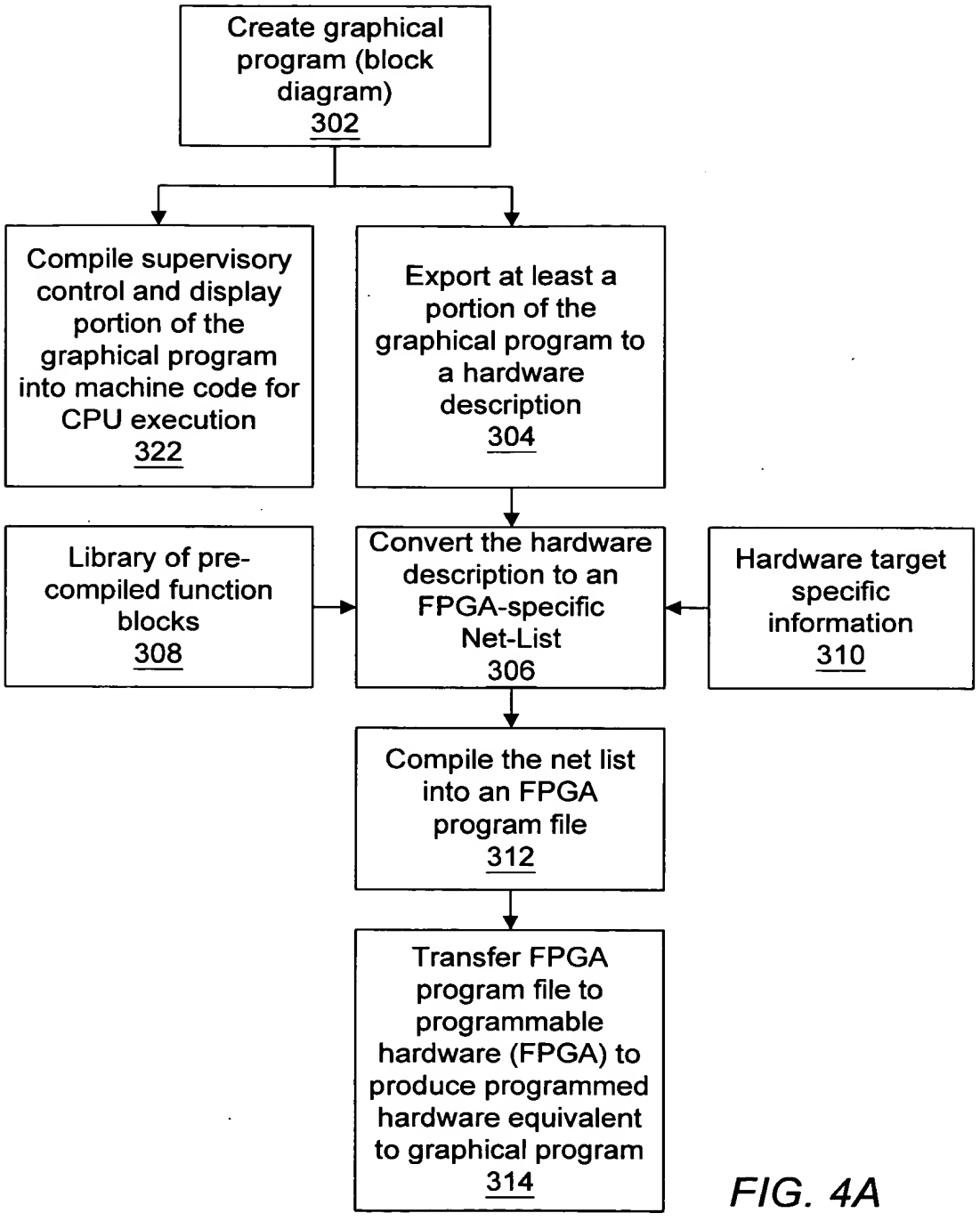
Create graphical program (block diagram) 302
Compile supervisory control and display portion of the graphical program into machine code for CPU execution 322
Export at least a portion of the graphical program to a hardware description 304
Library of pre-compiled function blocks 308
Convert the hardware description to an FPGA-specific Net-List 306
Hardware target specific information 310
Compile the net list into an FPGA program file 312
Transfer FPGA program file to programmable hardware (FPGA) to produce programmed hardware equivalent to graphical program 314

FIG. 4A

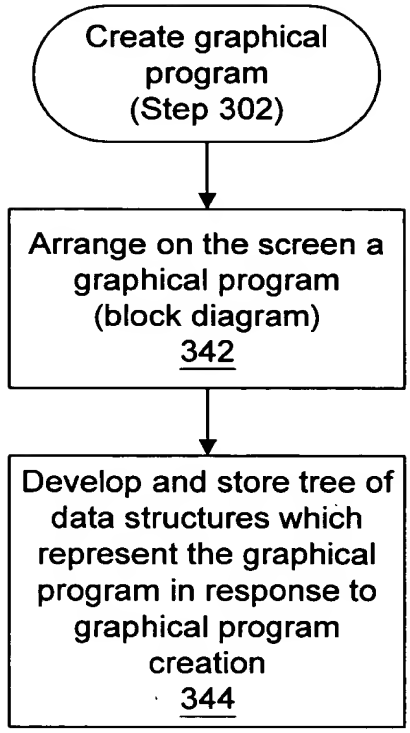
Create graphical program (Step 302)
Arrange on the screen a graphical program (block diagram) 342
Develop and store tree of data structures which represent the graphical program in response to graphical program creation 344

FIG. 5

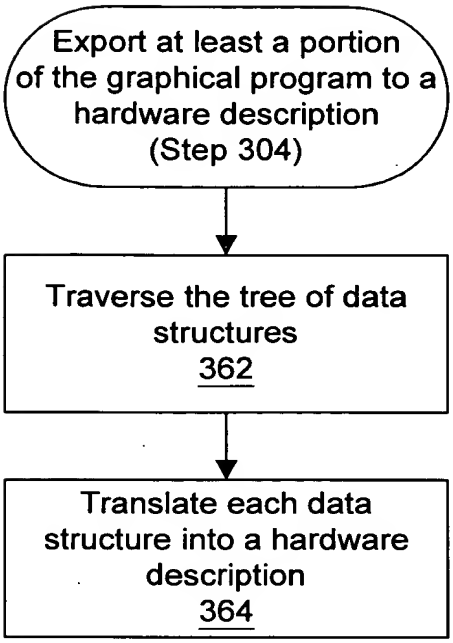
Export at least a portion of the graphical program to a hardware description (Step 304)
Traverse the tree of data structures 362
Translate each data structure into a hardware description 364

FIG. 6

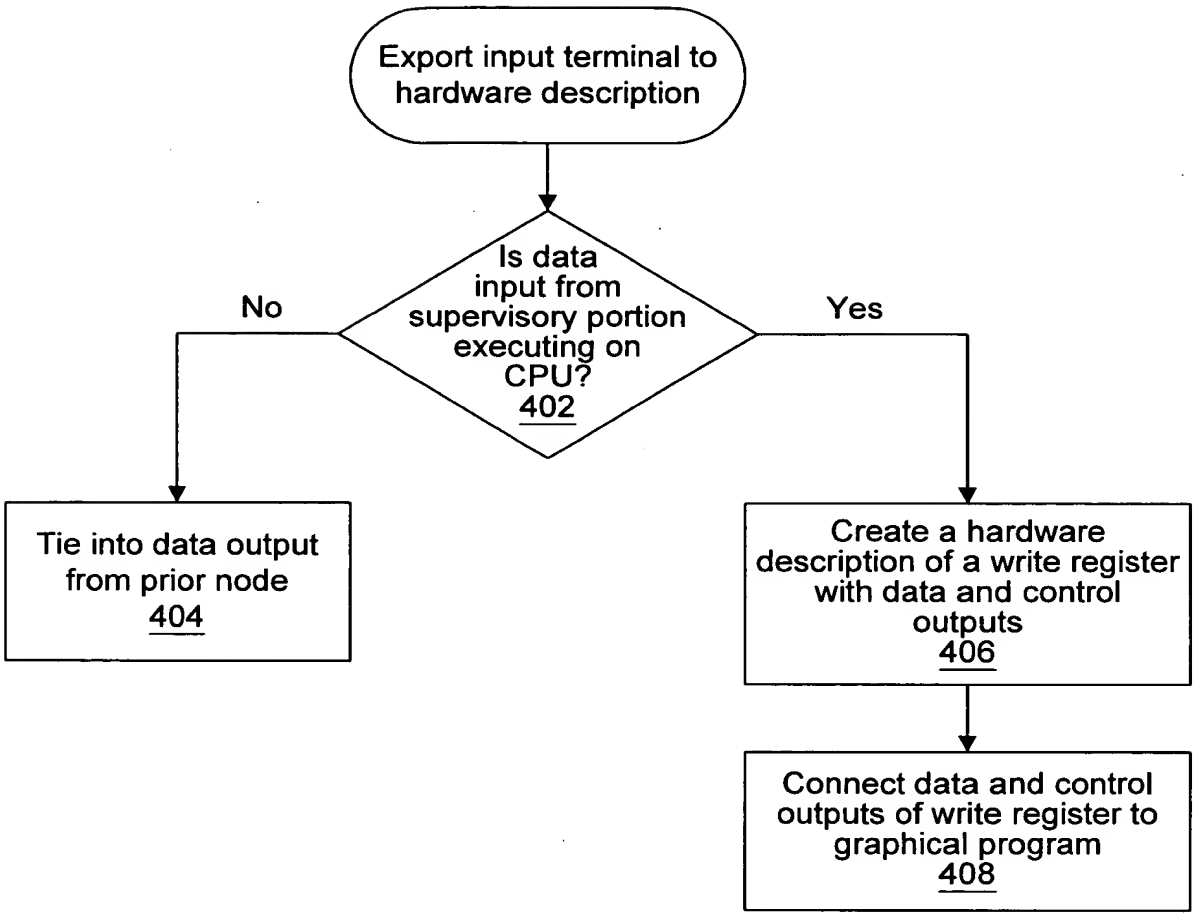
Export input terminal to hardware description
Is data input from supervisory portion executing on CPU?
402
No
Yes
Tie into data output from prior node
404
Create a hardware description of a write register with data and control outputs
406
Connect data and control outputs of write register to graphical program
408

FIG. 7

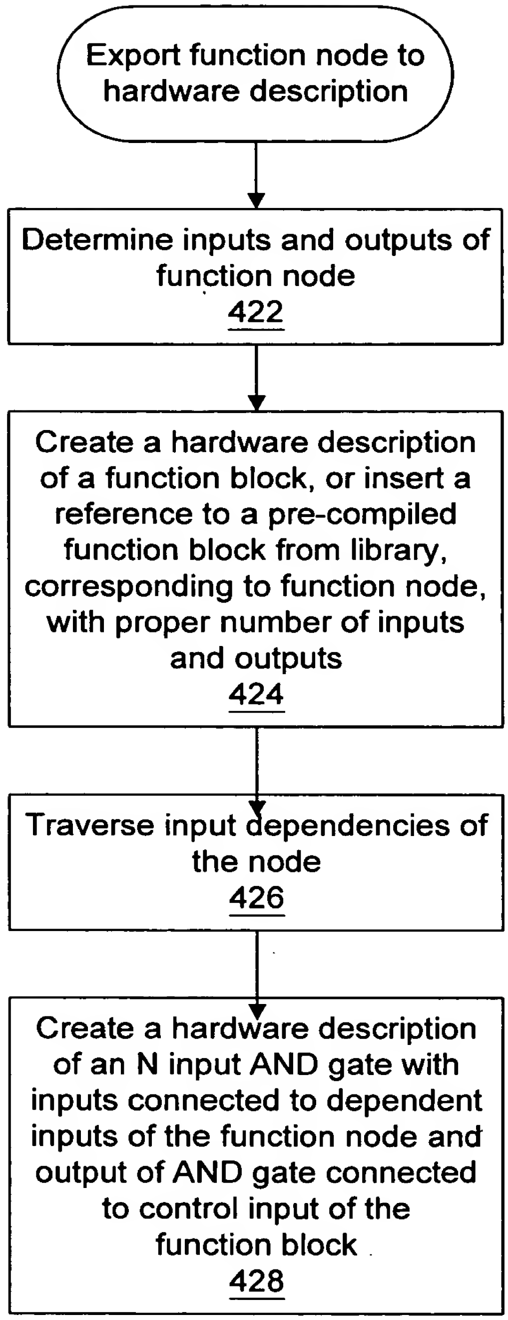
Export function node to hardware description
Determine inputs and outputs of function node
422
Create a hardware description of a function block, or insert a reference to a pre-compiled function block from library, corresponding to function node, with proper number of inputs and outputs
424
Traverse input dependencies of the node
426
Create a hardware description of an N input AND gate with inputs connected to dependent inputs of the function node and output of AND gate connected to control input of the function block
428

FIG. 8

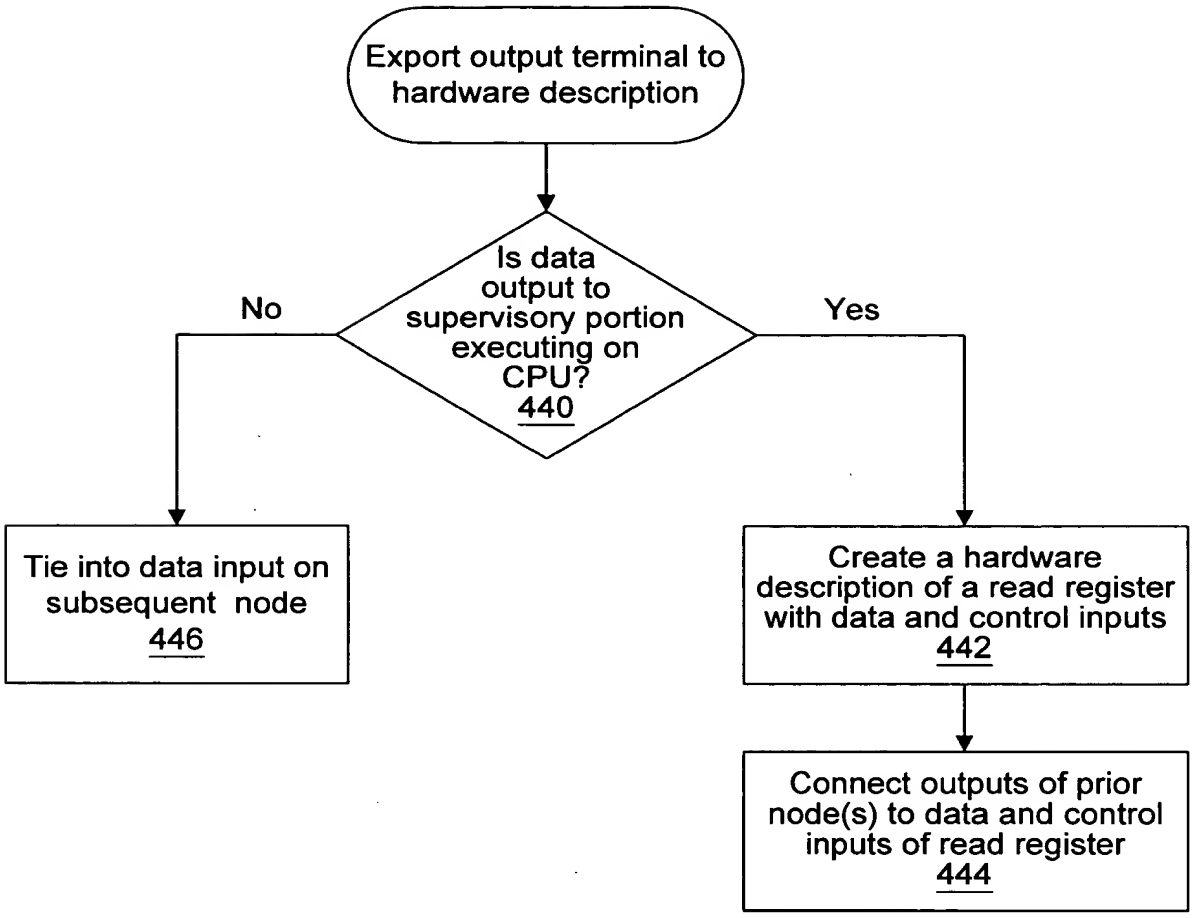
Export output terminal to hardware description
Is data output to supervisory portion executing on CPU?
440
No
Yes
Tie into data input on subsequent node
446
Create a hardware description of a read register with data and control inputs
442
Connect outputs of prior node(s) to data and control inputs of read register
444

FIG. 9

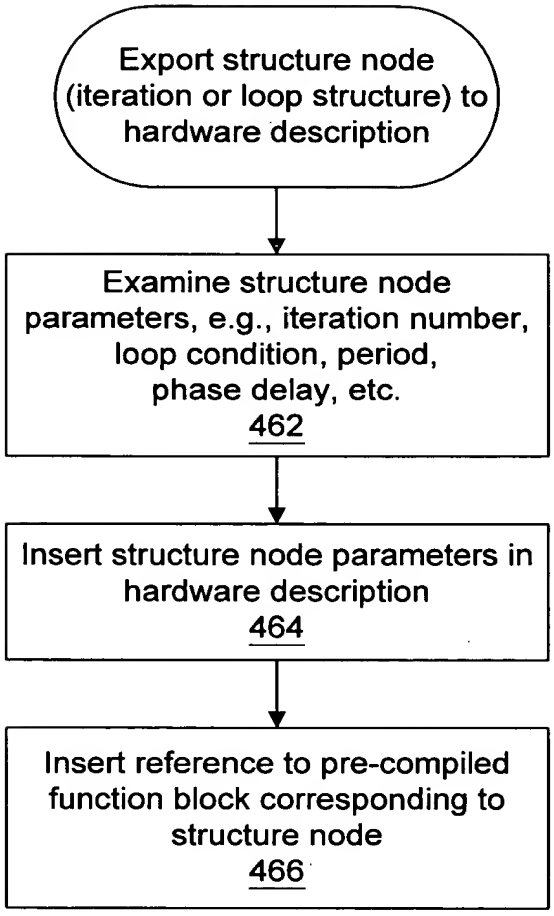
Export structure node (iteration or loop structure) to hardware description
Examine structure node parameters, e.g., iteration number, loop condition, period, phase delay, etc.
462
Insert structure node parameters in hardware description
464
Insert reference to pre-compiled function block corresponding to structure node
466

FIG. 10

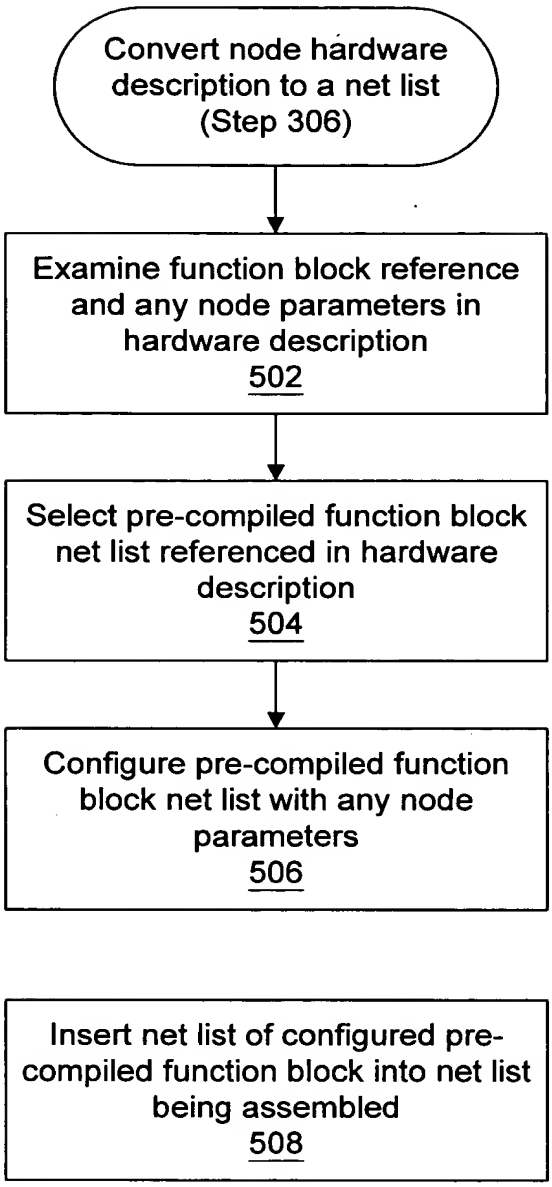
Convert node hardware description to a net list (Step 306)
Examine function block reference and any node parameters in hardware description 502
Select pre-compiled function block net list referenced in hardware description 504
Configure pre-compiled function block net list with any node parameters 506
Insert net list of configured pre-compiled function block into net list being assembled 508

FIG. 11

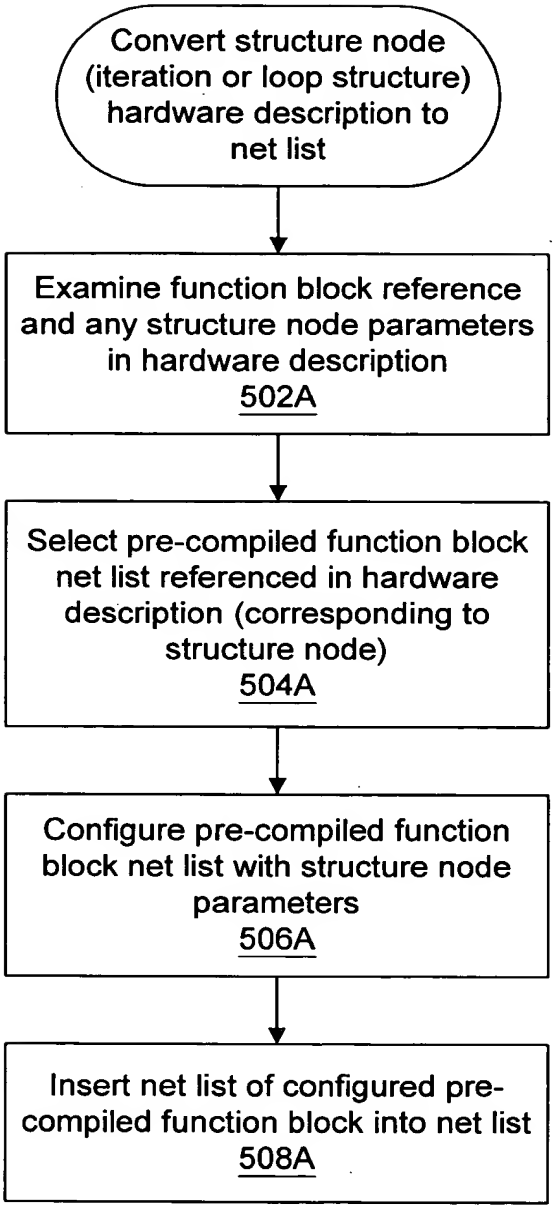
Convert structure node (iteration or loop structure) hardware description to net list
Examine function block reference and any structure node parameters in hardware description
502A
Select pre-compiled function block net list referenced in hardware description (corresponding to structure node)
504A
Configure pre-compiled function block net list with structure node parameters
506A
Insert net list of configured pre-compiled function block into net list
508A

FIG. 12

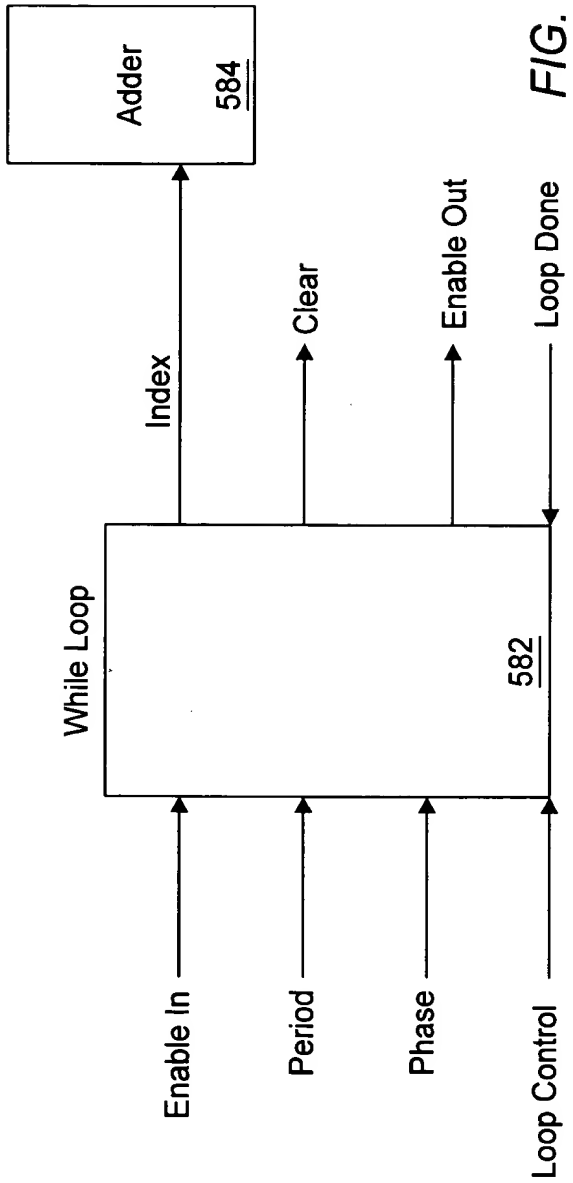
Adder
584
Index
Clear
Enable Out
Loop Done
While Loop
582
Enable In
Period
Phase
Loop Control

FIG. 13

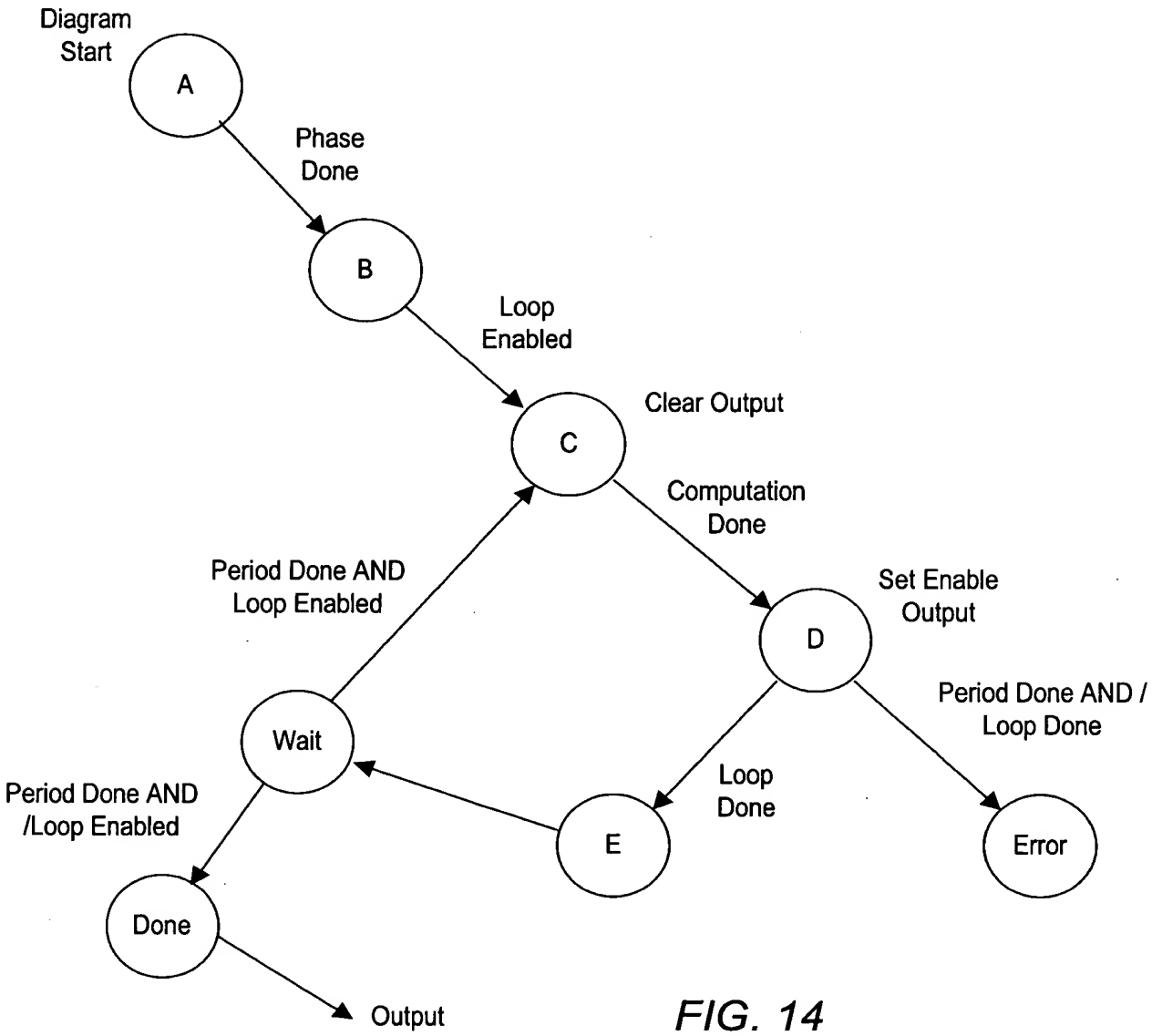
Diagram Start
A
Phase Done
B
Loop Enabled
C
Clear Output
Computation Done
D
Set Enable Output
Period Done AND / Loop Done
Error
Loop Done
E
Period Done AND Loop Enabled
Wait
Period Done AND /Loop Enabled
Done
Output

FIG. 14

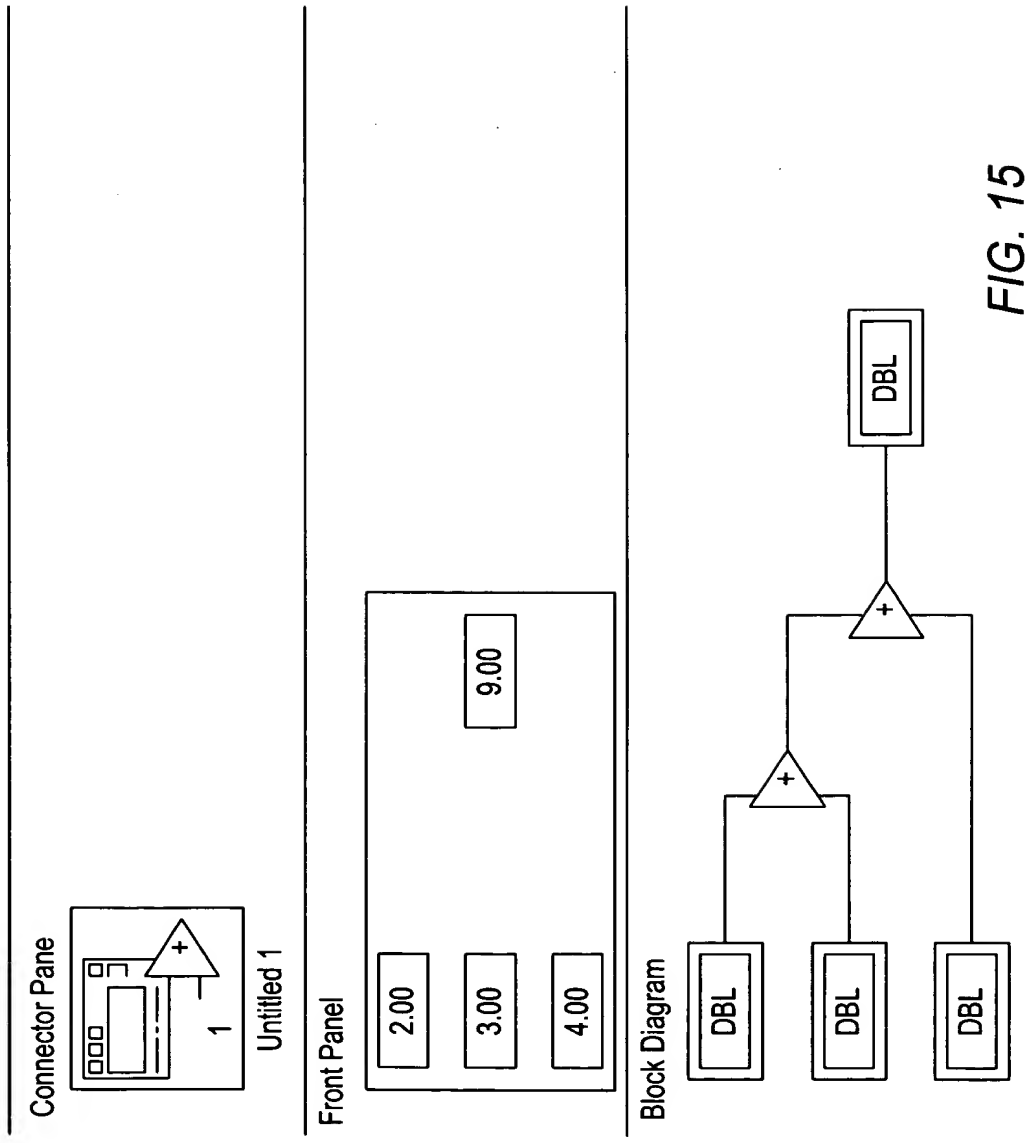
Connector Pane
1
Untitled 1
Front Panel
2.00
3.00
4.00
9.00
Block Diagram
DBL
DBL
DBL
DBL

FIG. 15

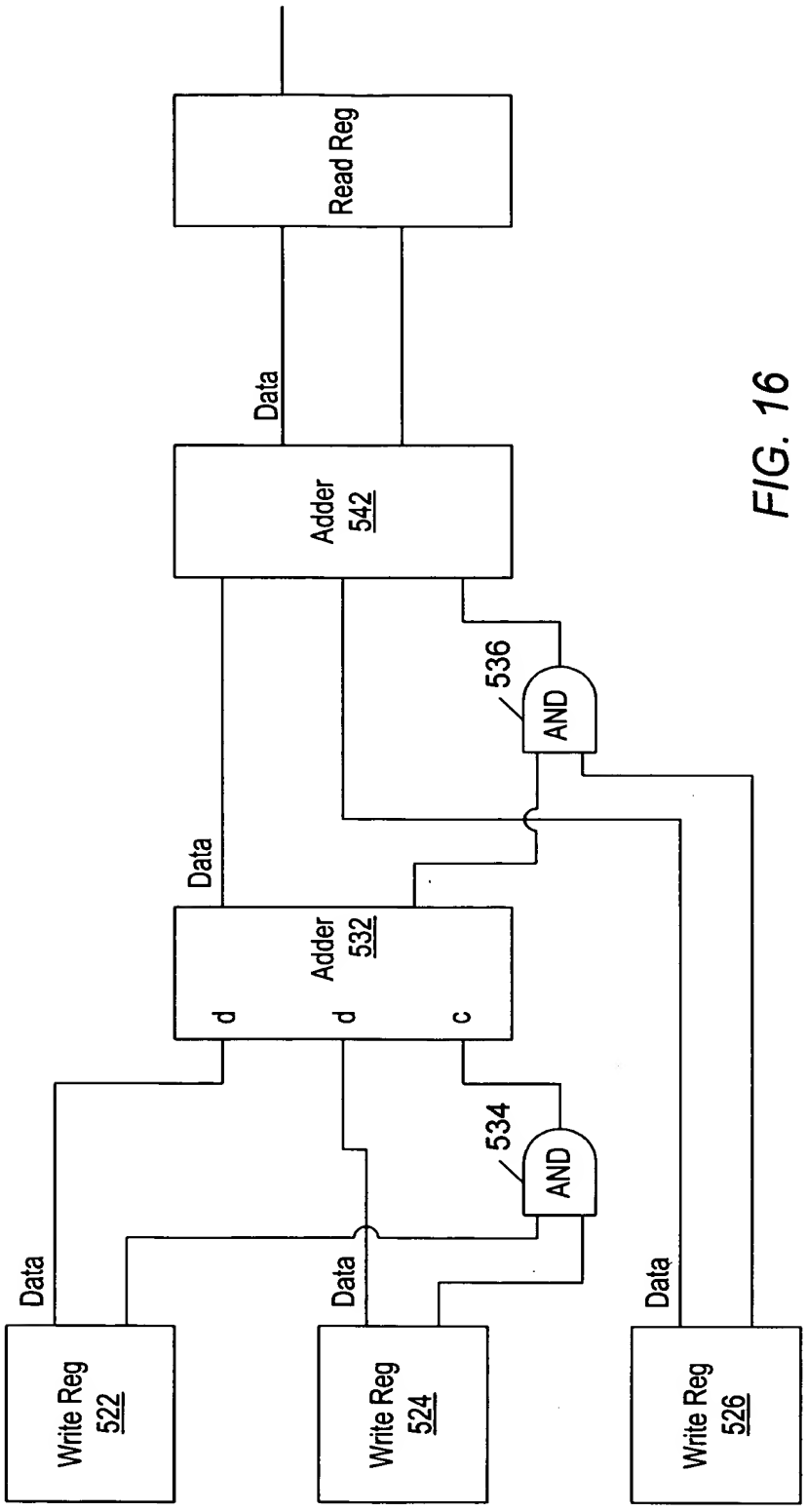
Read Reg
Data
Adder
542
536
AND
Data
Adder
532
d
d
c
534
AND
Data
Data
Data
Write Reg
522
Write Reg
524
Write Reg
526

FIG. 16

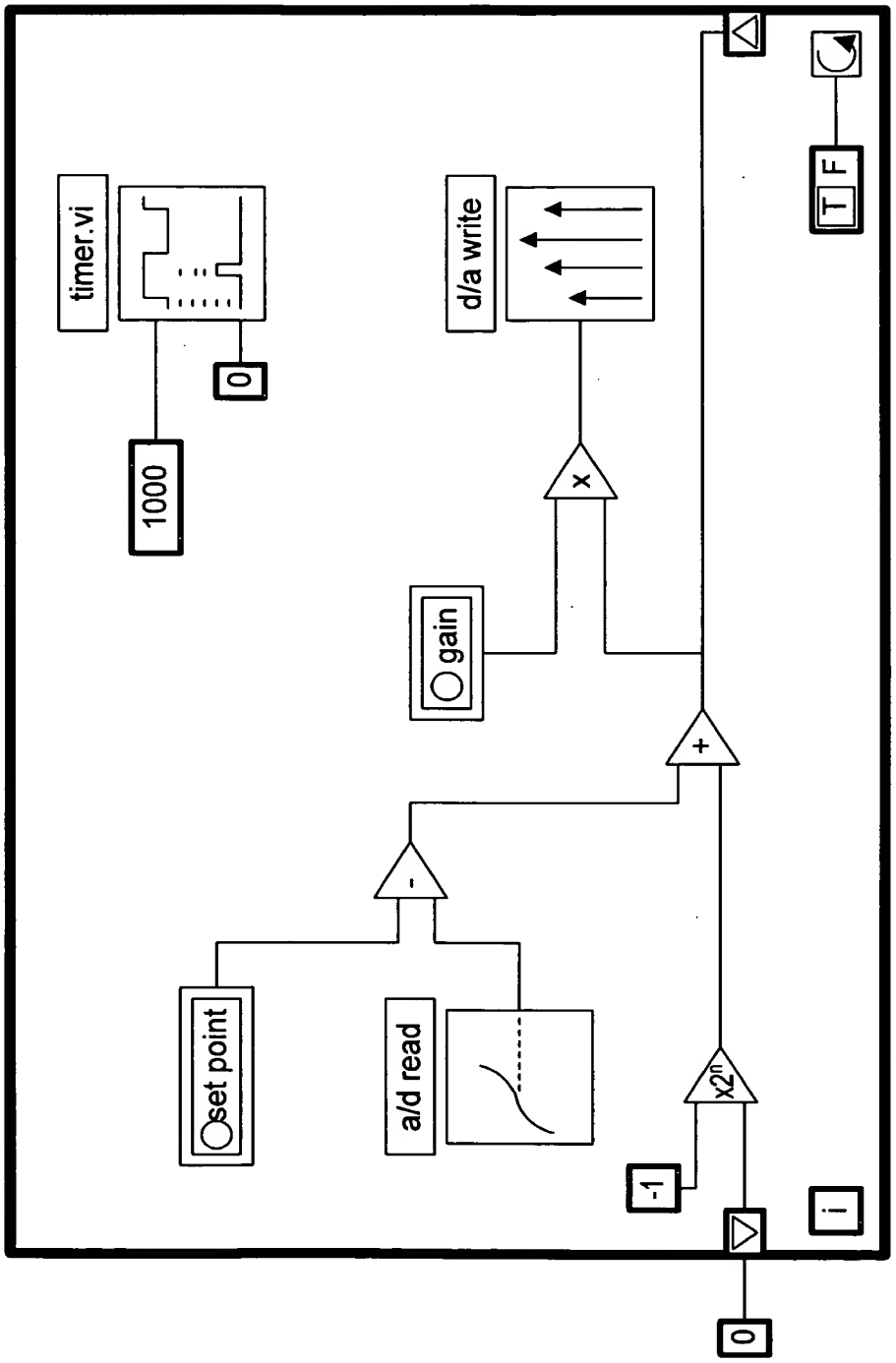
LabVIEW Diagram
timer.vi
1000
0
d/a write
gain
x
set point
a/d read
-
+
x2^n
-1
0
i
T F

FIG. 17

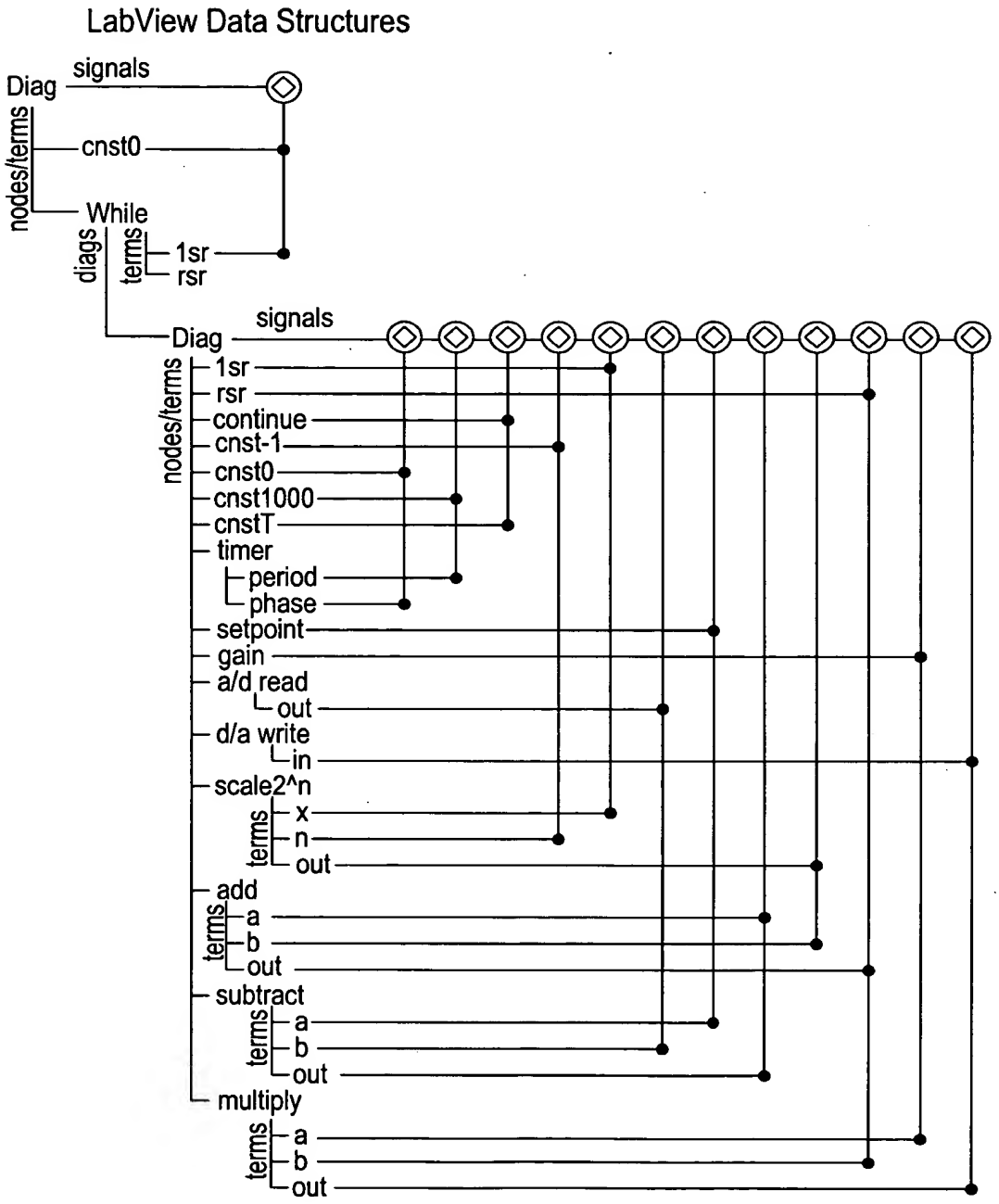
LabView Data Structures
Diag
signals
nodes/terms
cnst0
While
diags
terms
1sr
rsr
Diag
signals
nodes/terms
1sr
rsr
continue
cnst-1
cnst0
cnst1000
cnstT
timer
period
phase
setpoint
gain
a/d read
out
d/a write
in
scale2^n
terms
x
n
out
add
terms
a
b
out
subtract
terms
a
b
out
multiply
terms
a
b
out

FIG. 18

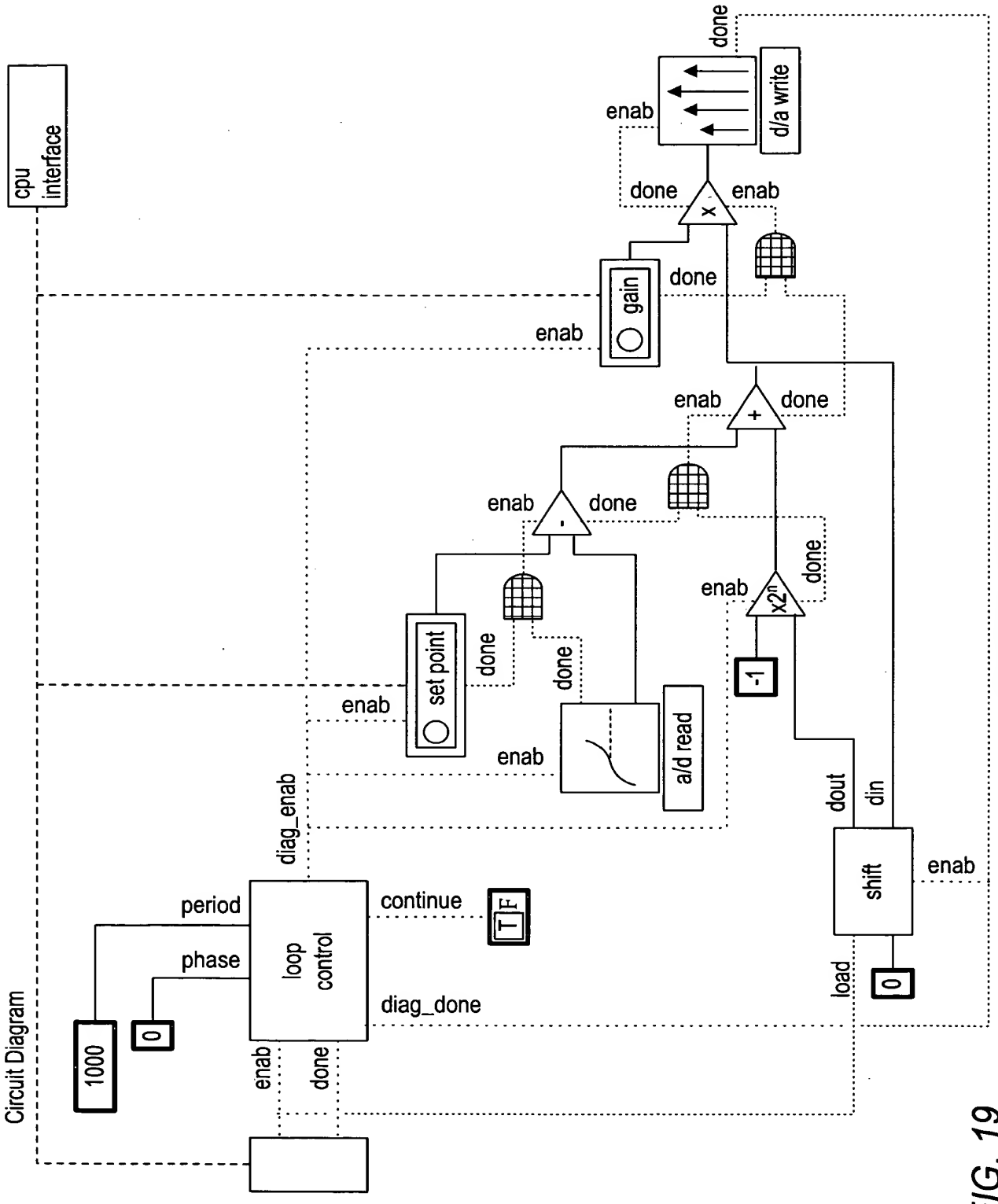
cpu interface
done
d/a write
enab
done
enab
x
gain
done
enab
enab
done
+
enab
done
-
done
enab
x2^n
done
-1
set point
done
enab
done
a/d read
enab
diag_enab
dout
din
shift
enab
period
continue
T F
loop control
phase
load
0
diag_done
1000
0
enab
done
master clock connects to all
Circuit Diagram

FIG. 19